METHOD ON SCAN CHAIN REORDERING FOR LOWERING VLSI POWER CONSUMPTION

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to a method for reordering a scan chain, and more particularly to a method for reordering a scan chain that minimizes the peak power consumption of Very Large Scale Integration (VLSI) Circuits.

2. Description of Related Art

Along with VLSI Circuits designed more complex, higher density transistors and lower power consumption components are used widely. Designing a lower power consumption VLSI circuit is the latest trend.

In recent years, a topic for discussion of the Design for Testability (DFT) of VLSI against the power dissipation has been widely regarded. A general designed circuit is operated in two modes: Normal Mode and Test Mode. In the test mode, the test patterns for testing combinatory logic circuit are stored in the scan register of system. Some of the test patterns may not appear in the normal mode at all. In other words, the potential conversion of register that may not happen in the normal mode possibly and happen in the test mode. Therefore, the test pattern in the test mode will lead to high power dissipation in the circuit of register. In another aspect, the test pattern is generated by Automatic Test Pattern Generator (ATPG) that is designed with DFT and will test the majority of circuits as possibly as it can and make the potential of the circuits frequently convert, thereby causing the condition circuit to be more deteriorated.

It is noteworthy that an oversized peak value of power dissipation will lead to a malfunction of the circuit during testing and namely, a chip normally operating in the normal mode may not be qualified by ATPG. There are various ways of improvement of reducing the power dissipation in the testing mode. Some conventional technologies (R. M. Chou, K. K. Saluja, and V. D. Agrawal, "Scheduling tests for VLSI systems under power constraints," IEEE Trans. VLSI, vol. 5, no. 2, pp. 175-184, 1997 and S. Wang and S. K. Gupta, "ATPG for heat dissipation minimization during test application," in Proc. IEEE Int. Test Conf., 1994, pp. 250-257) are used ATPG to create the optimum test patterns capable of reducing the power dissipation.

Further, re-ordering the Scan Chain register can also effectively reduce the power dissipation at the time of the potential conversion. As shown in figure 1A, if the test pattern data, 0101, is input to a 4-bit scan chain, ABCD, then it must take 4 times of shifts during total 10 times of the potential state conversion occur, wherein the potential state conversion of each bit occurs in the case of the last shift. If the re-ordered scan chain is BDAC, as shown in figure 1B, only 2 times of potential state conversion occur in the course of 4 times of shifts. A conventional technology (V. Dabholkar, S. Chakravarty, I. Pomeranz, and S. Reddy, "Techniques for minimizing power dissipation in scan and combinational circuits during test application," IEEE Trans. CAD, vol. 17, no. 12, pp. 1325-1333, 1998) provides two algorithms: Random Ordering and Simulated Annealing. However, if there is much test pattern data and there are large amounts of registers, ordering of a large number of registers is necessary so as to highly reduce the power dissipation as

possibly as it can, thereby causing uneconomical situation. However, simulated annealing an initial state that possibly is close to minimum power dissipation, or else it may take long time to perform the algorithm, which is not practical. Regarding this problem, this invention provides a research on scan chain ordering that fast meets the limits of design specifications. Also, still another conventional technology (O. Sinanoglu, I. Bayraktaroglu, and A. Orailoglu, "Scan power reduction through test data transition frequency analysis," in Proc. Int. Test Conf., 2002, pp. 844-850) is provided to insert an inverter into the parts of the positions of the scan chain, thereby reducing the probability of the potential conversion for a reduction of power dissipation. However, the insertion of the inverter will change the circuit placement formerly completed in the physical design of VLSI circuit, so that this practice is not involved in the research field of this invention. Next another conventional technology (S. Ghosh, S. Basu, and N. A. Touba, "Joint minimization of power and area in scan testing by scan cell reordering," in Proc. IEEE Computer Society Annual Symposium on VLSI, 2003, pp.) seeks for an optimum scan chain ordering using Greedy Algorithm, and considers the connection distance between the power dissipation and the registers. Supposing that the coordinates of the two registers are (x1, y1) and (x2, y2), respectively, and then $|x1-x2|+|y1-y2|$ is given for Manhattan Distance between the two registers.

In addition to the two conditions, as mentioned above, the limitations of the total connection length of scan chain, namely total length of distance between registers, is considered. Again, seeing from the technologies, hereinbefore, a fixed value is given for the power dissipation of each of the two registers in the scan

chain, and hence to reduce the peak value of the power dissipation is to cut down the number of times of the potential state conversion. It is considered in the present invention that the practical power dissipation value of register is not fixed, so that a small number of times of potential state conversion unnecessarily mean small power dissipation.

SUMMARY OF THE INVENTAION

The test pattern data is in a proper order input from the outside of the scan chain into the inside of each of the registers for testing the combinatory logic circuit. When an N-class register is included in a scan chain, the test pattern data must pass through N clock period to shift its value in a proper order and to store the test pattern data in a corresponding one of the registers. In this process, the shift may cause power dissipation when one of the states, 0-1 or 1-0, of the shift registers is changed.

This method of the present invention is to re-order the corresponding positions of each of the registers on the scan chain for reduction of the peak power dissipation. The algorithm tool according to the present invention not only can match with the current design flow for VLSI circuit to fast determine the proper order of the registers on the scan chain, but also can meet 3 following design conditions: (1) peak value of power dissipation at potential conversion of register, (2) the maximum value of total connection length of scan chain, and (3) the maximum value of connection distance between two adjacent registers. The scan chain buffer data and the test pattern data are input, and finally ordered the scan chain buffer data and the test pattern data that meet all conditions are output.

This method of the present invention, hereinbefore, is characterized that (1) an integrated data structure storing buffer and various delay information are built to facilitate data access in the process of program computation, and (2) a Feasible Solution of a Clock Tree can be promptly determined, wherein If the Clock Tree is not provided with any feasible solution, the optimum algorithm will not be performed any more, and the determined results are output for reference, (3) some Heuristic concepts instead of Exhaustive Search algorithm are applied to solve the problem, thereby saving time for optimal solution, and (4) within the range allowable by equipment, the algorithm tool according to the present invention is capable of processing a quite large circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1A shows a simple embodiment illustrating a scan chain before arranged;

Fig. 1B shows a simple embodiment illustrating a scan chain after arranged;

Fig. 2 shows an IC design and layout flow chart according to a conventional technology;

Fig. 3 shows an I/O block diagram of an algorithm tool according to a particular embodiment of the present invention; and

Fig. 4 shows a flow chart explaining a database of registers adjacent to each other according to the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Figure 2 shows an IC design and layout flow chart according to a conventional technology. Step 1 for placement and step 4 for winding are the traditional IC layout steps, wherein timing and noise optimization can be considered together. At step 2, Clock Tree Synthesis is performed to meet Clock Delay and Clock Skew. Next, at step 3, the scan chain re-ordering is performed. At this time, all circuits layout is completed, the scan chain registers are arranged in order according to only design specification, and the finally winding is performed.

Figure 3 shows an I/O block diagram of an algorithm tool according to a particular embodiment in accordance with the present invention. The scan chain register circuit data 301 defines the name of each of the registers, the 2D coordinates, and the power dissipation value. The 2D coordinates can provide Manhattan distance for algorithm. After a unit of test pattern data being input, every time a shift is made, and then the total power dissipation of the registers of which the potential is converted and calculated until the test pattern shift stops and then the peak value of power dissipation is gained. In the test pattern data 303 of scan chain, if an M unit of the test pattern data is provided, the maximum is picked again from the peak values of the corresponding M- unit power dissipation.

For simplicity, it is supposed in the present invention that (1) the defaults of the potential state of each of the registers are 0 before a first unit of the test pattern data is input, and (2) after the former unit of test pattern data being completely shifted and output, the values of each of the registers are equal to those of registers at the input of scan chain, and at this time another unit of new test pattern data is input. We assume that an algorithm of the power dissipation is

performed only when the potential conversion occurs in scan chain. Three limited conditions are set in the design specification for data 305: (1) peaking value of the power dissipation at the time of potential conversion of register, (2) the maximum of total connection length of scan chain, and (3) the maximum of connection distance between two adjacent registers.

Generally speaking, the Exhaustive Search is quite easy to get an optimal solution; that is to say, all registers are sequentially arranged and a unit of the optimal arrangement order is found to meet all the limited conditions. However, the main disadvantages are the cases that (1) *N!* type(s) of arrangements are provided for *N* unit(s) of registers, and the maximum power dissipation must be compared with each arrangement, so that the algorithm is largely complicated, and (2) If there is no feasible solution that meets the limited condition(s), the determination is not made until the N! type(s) of the arrangement(s) is/are implemented.

As described above, fore regarding the problem, the developed algorithm tool according to the present invention provides as possibly as it can prompt the determination of a feasible solution, and quick and effective search for an optimal solution. The main step of the algorithm tool includes three items as follow:

1. According to the maximum limited distance between the two adjacent registers, first at step 1, in Fig. 3, it is determined whether a Feasible Solution meeting the limit condition is provided. If any, at step 2, in Fig. 3, each register is adjacent to a register that is searched, and a database is built to store the information. If none, no feasible solution

321 meeting the condition is provided;

2. An event 311 impossibly meets the maximum limited distance and the maximum, and the total length of the scan chain is deleted; and
3. For the given test pattern, the arrangement order 313 of the register on the scan chain is made for a reduction of the peak value of the power dissipation, and it is determined whether the peak value limit of the power dissipation and the limit condition 315 of maximum total length for scan chain connection accord. If yes, the updated scan chain arrangement 317 and the corresponding scan chain test pattern data 319 are output, and If not, no feasible solution 321 meeting the limit condition of design is provided.

The present invention will be described in more details hereinafter.

Establishment of a Database of Register Adjacent to Each Other

A memory space is used to build a register database that meets the maximum distance between the two registers adjacent to each other. In the course of arrangement of each of the registers, the registers possibly adjacent to each other are determined according to the limit condition. If there are a large number of the registers in the scan chain, it takes much time in one-by-one search. Therefore, it is required to pre-build a group database of registers adjacent to each other. At the time of the arrangement, the search field can be narrowed, thereby saving much time in search.

To effectively build a database, the following three stages will pass in the processes, as shown in Figure 4.

1. The distributed areas on the coordinates of all registers are divided into the form of grid, and a grid 403 attributed to each register is stored; use D representing the maximum limit of the distance between two registers that are adjacent to each other. The distributed areas of registers are divided into grids of $2D$ in length and width. When a scan chain register file is read, the coordinates of each of the registers are saved at the same time. In addition, the positions of each of the registers in the grid are unnecessarily fixed in the center so that the two adjacent registers are possibly in the circumference of the grid and their coordinates must also be saved. For example, in case of D=5, if the register coordinates are (37, 52), then the register stays in a grid (4, 6). Said register stays at lower right-hand corner, so the corresponding adjacent registers be in grids (5, 6), (4, 5), and (5, 5);
2. A register 405 falling in each grid is recorded; and
3. An adjacent registers group 407 according to the maximum distance limit in the grid and in the circumference of the grid is found and recorded.

However, if the maximum limit of the distance between the two adjacent registers is over, it is not proper to build such a database for search request. The higher maximum limit of distance is required, the more the registers adjacent to each other is employed, and also the more the data must be stored, the more the data is searched and the time is taken. Consequently, in the condition of invalid search, the memory space is wasted without any reason. Hereby, in order to solve

this problem, in the present invention based on the statistics, only when the amount of grid is larger than or equal to 9 (grids), a database of the adjacent registers is built, or else, a search in an entire area will be made.

An event impossibly meeting the maximum limited distance and the maximum, the total length of scan chain is deleted.

First, an event impossibly meeting the maximum limit of distance is considered. According to the database of the adjacent registers that is built in the former step, the following particular situations can be concluded.

Existence in a register without any corresponding group of the adjacent registers: indicates that the design is provided with no feasible solution. Existence in a register with only an adjacent register indicates that the register must be the output terminal of this scan chain, and its adjacent register is second in arrangement order.

Existence in two registers with only an adjacent register: both of the two adjacent registers indicate no feasible solution is given. For example, if the register *A1* is adjacent to the register *A*, then the register *B1* is adjacent to the register *B*. If *A* is *B1*, then it is inferred that *A1* is *B*. Except *A* and *B*, no registers are adjacent so that no solution is given.

Two registers are different from each other and indicate that one register can be made as the input of scan chain, and the other as the output.

At least four registers with only an adjacent register indicate that no feasible solution is given. Except the I/O terminals of the scan chain, no places allow the register, so no feasible solution is given.

Next, the event not meeting the maximum, the total length limit of the scan chain is deleted. At this step, the best case and the worst case are respectively estimated for the scan chain length. Regarding any of the registers I, the distance D_i^{min} closer to the other registers, the distance D_i^{max} further from the other registers, and the distance D_i^{avg} equidistant from the other registers are estimated. If $L^{min}= \Sigma_i D_i^{min}$, $L^{max}= \Sigma_i D_i^{max}$, and $L^{avg}= \Sigma_i D_i^{avg}$ are made, then through the estimation, the scan chain length is given L^{min} for the best case, while the scan chain length is given L^{max} for the worst case. The actual scan chain length is not probably L^{min} or L^{max}, but the length falls within the two margins, so that a judgment can be made between the two margins. It is assumed that the total limit of the length of the maximum scan chain is L_{lim} and the two lengths are compared with each other for estimation, and then conclusion is made as follows:

- $L_{lim}<L^{min}$: no feasible solution given;
- $L^{min} <= L_{lim} < L^{max}$: at the time of the arrangement of the scan chain register at a next step, in addition to a search for a combination of the peak values in the adjacent registers so as to reduce power dissipation, a case beyond the total limit of length of the maximum scan chain also being taken into consideration so that registers must be arranged to shorten the scan chain on the occasion; and
- $L^{lim}>L_{max}$: at the time of arrangement of the scan chain registers at a next step, the total limit of length of the maximum scan chain not being taken into consideration but a search of a set of peak values in the adjacent registers to reduce power dissipation.

Arrangement of the registers on Scan Chain

When the shift of a test pattern on the scan chain is observed, it can be found that more the register is close to the output of scan chain, the more groups of the shift registers of the opposite test pattern will pass by. Thus, the state conversion of register 0-1 or 1-0 may be caused for many times in the course of the shift. In the algorithm tool according to the present invention, registers at the output of the scan chain are in advance set, and then the registers are recursively arranged in order towards the input terminal. The point is to decide a next optimal register to be arranged an optimal register of the output terminal.

A peak value of the power dissipation is not given in the calculation until the registers on the entire scan chain is fully arranged, also, the calculation is enormous so that an actual value of the power dissipation cannot be given in the course of recursive arrangement. In the aspect of the reduction of the power dissipation peak, it is expected in the method of the present invention that the number of times of the register state conversion caused in the period of shift is reduced, which is a concept on the statistics for an average in order to avoid an enormous peak value of the power dissipation at the time of huge state conversion. In order to reduce the calculation loading at the same time, the algorithm tool according to the present invention uses a logical XOR calculation to every time sort out a next optimal register in a set of registers having not been arranged in the course of arrangement so that the opposite test patterns can be a little different from the test patterns of registers so far having been arranged, thereby reducing the probability of register state conversion in each shift.

For example, the test patterns with respect to *A*, *B*, *C*, and *D* are listed below, and it is assumed that *A* has been arranged.

A	B	C	D
0	1	0	1
1	0	1	1
1	1	0	0
0	1	0	1
1	0	1	0

First, B, C, and D respectively corresponding to A are calculated through XOR, and the minimum is used as an adjacent register of A. In case of XOR(B,A)=4, XOR(C,A)=1, and XOR(D,A)=4, C is adjacent to A. Next, B and C respectively corresponding to C are calculated through XOR, and the minimum is used as an adjacent register of C; in case of XOR(B,C)=5 and XOR(D,C)=2, D is adjacent to C, and B is the last one remaining. Thus, BDCA is the arrangement in order made from input to output on the scan chain.

Then, a selection of a register at the output terminal is considered. The test pattern opposite to the register at the output will continuously affect the state conversion of each of the shift registers and the arrangement of the scan chain. However, generally speaking, they cannot be tested one by one for a suitable register at the output. Hereon, some experiences are used to help in judgment.

According to the last step, the special case of the built adjacent register database is used so that a register is existed with an adjacent register only, and two registers are existed respectively with an adjacent register only and the two registers are different from their adjacent registers.

If no special conditions occurred, the minority of the adjacent registers among all registers is used as the registers at the output. Thus, in the case, the register cannot find an adjacent register in the scan chain is reduced, thereby facilitating the algorithm in time saving.

No provision of an adjacent register database indicates that there is no strict limit of the maximum distance between the adjacent registers, and thus the probability that the register cannot find any adjacent register in scan chain is lower. At this time, of all registers, a register of the maximum power dissipation is used as an output terminal, and that less different from the test pattern is used as an input terminal, thereby effectively lowering the impact of the register of maximum power dissipation to the peak value of power dissipation through full design.

Other Special Cases

Some special cases happening in the foregoing algorithm cannot be solved, so that the conclusion is made below.

Ordering of the registers on the scan chain simply through the reduction of the peak value of the power dissipation only may be contrary to the limit of the maximum scan chain length. To solve the problem, the time for algorithm tool to order the scan chain must be determined best of all through shortening of the distance to the registers for conformability with the limit of maximum length. In the preferred embodiment of the present invention, an experience is used for estimation.

After the registers being arranged each time through the results given from algorithm with XOR, the remaining length compared with the maximum

length is estimated, the number of registers not arranged is divided, and finally, an average remaining distance is given.

Next, estimation of the margin around the average remaining distance is considered. The average estimation of the two proximal distance $D^{min}=L^{min}/\Sigma_i i$ is ideal, while average estimation of the averaged distance $D^{avg}=L^{avg}/\Sigma_i i$ is actual, thus, the minimum between $10*D^{min}$ and $(D^{min}+D^{avg})/2$ is taken in the method of the present invention for estimation. Once the averaged remaining distance is less than the estimative value, the next registers are arranged very adjacent to each other.

A case that the registers not arranged existing in any of the registers not found adjacent intuitionally replace with another register. If no other registers exist, it is known that the arrangement of the former one register or several registers arranged is not proper, thus, the sequence of the scan chain registers formerly have been arranged must be again considered like DFS or Branch-and-Bound. However, in this estimation, the algorithm loading and the memory space required are too large to deal with a scan chain with a great lot of registers. Thus, for fear of no adjacent registers not arranged, in addition to a next register selected through XOR, a register adjacent to maximum registers not arranged must be found and recorded.

In short, in the present invention, a method of reordering a scan chain for the design of testability on VLSI with low power dissipation is provided to work with the current design flow for VLSI, to promptly determine the sequence of registers on a suitable scan chain, and to meet three limited conditions in the design specification: (1) peak value of power dissipation at the time of potential

conversion of register, (2) the maximum of total connection length of scan chain and (3) the maximum of connection distance between adjacent two registers. The main steps of performing the algorithm tool in accordance with the present invention include: to determine whether a Feasible Solution meeting the maximum limit of distance between the two registers adjacent to each other being provided, if yes, a database of registers adjacent to each other is built; if not, no feasible solution meeting the limit condition of design is provided. An event impossibly meets the maximum limited distance and the maximum and the total length of the scan chain is deleted. For the given test pattern, the registers on scan chain are re-ordered and it is determined whether the peak value limit of power dissipation and the limit condition of maximum total length for scan chain connection accord, if yes, the updated scan chain arrangement and the corresponding scan chain test pattern data are output; if not, no feasible solution meeting the limit condition of design is provided.

As described above, only operational principles are given that does not limit the present invention. Although the invention has been explained in relation to its preferred embodiment, it is to be understood that many other possible modifications and variations can be made without departing from the spirit and scope of the invention as hereinafter claimed.